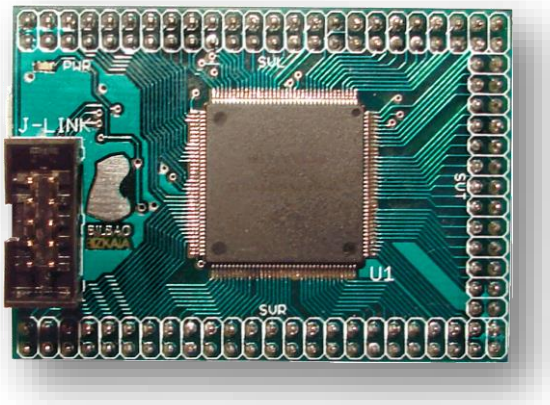
BILBAO BIZKAIA minimodule



Wrocław University of Technology

Wrocław, 17.12.2013

The module along with the documentation have been developed by: Mateusz Cholewiński, Michał Dziergwa, Paweł Kaczmarek, Jan Kędzierski, Marek Wnuk.

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Wrocław 2013

The documentation consists of this manual and a project created using EAGLE ver. 6.5.0. software from CadSoft. This project can be obtained from the authors of the module. It can be used for educational purposes only.

Bilbao is a city in Spain, the capital of the province of Biscay. The population proper is just over 372,000. Nowadays, Bilbao is a vigorous service city that is experiencing an ongoing social, economic, and aesthetic revitalisation process, started by the iconic Bilbao Guggenheim Museum, and continued by infrastructure investments.

Contents

1. Introduction

The minimodule described in this document is based on a 32-bit MK60FX512 microcontroller from Freescale's Kinetis family [1]. It contains all the necessary components required to communicate with the microcontroller and allow the proper operation of the on-board modules (JTAG and USB connector, 50 MHz/32 kHz clock sources, diodes, resistors, capacitors, inductors).

The main purpose of this project was to design a small and flexible standalone module that would enable the use of the wide range of K60 microcontroller's capabilities in a broad spectrum of educational applications. The final version of the board can be seen in Fig 2 and Fig 1.

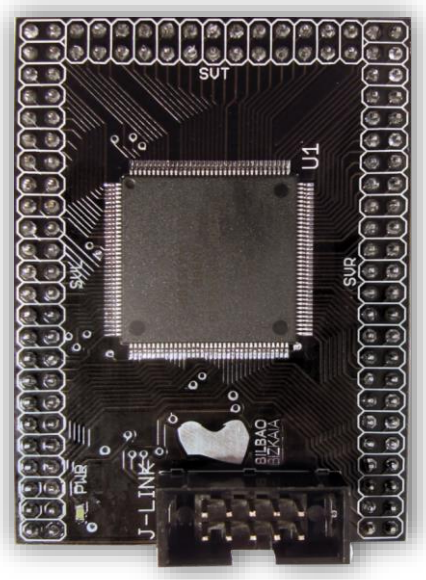


Fig 2 Assembled board - top

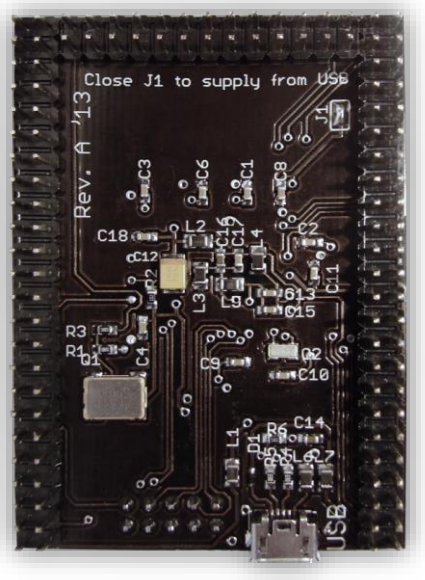
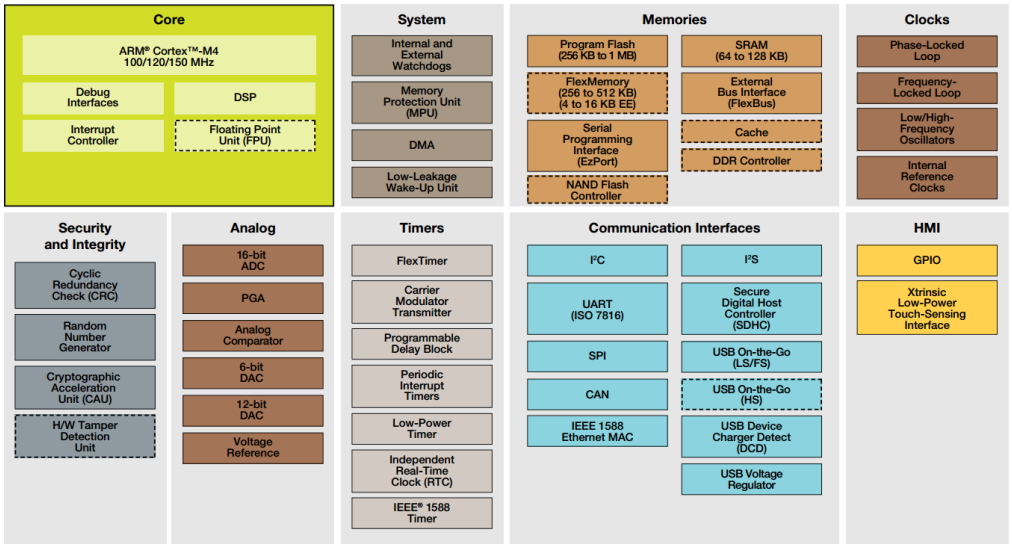


Fig 1 Assembled board - bottom

2. Overview

The Kinetis MCU portfolio consists of multiple pin-, peripheral- and software-compatible MCU families based on the ARM® Cortex™-M4 core [2]. Families are built from innovative 90 nm thin-film storage (TFS) flash technology with unique FlexMemory (EEPROM) capability, and offer industry-leading low power and mixed signal analog integration. The K60 MCU family includes IEEE® 1588 Ethernet, Full- and High-Speed USB 2.0 On-The-Go with device charger detect capability, hardware encryption and tamper detection capabilities. Devices start from 256 KB of flash in 100 LQFP packages extending up to 1 MB in a 256 MAPBGA package with a rich suite of analog, communication, timing and control peripherals. High memory density K60 family devices include an optional single precision floating point unit, NAND flash controller and DRAM controller.



3. Features of MK60FX512VLQ15

- **Operating Characteristics**
  - Voltage range: 1.71 to 3.6 V
  - Flash write voltage range: 1.71 to 3.6 V
  - Temperature range (ambient): -40 to 105° C

- **Performance**
  - Up to 150 MHz ARM Cortex-M4 core with DSP instructions delivering 1.25 Dhrystone MIPS per MHz

- **Memories and memory interfaces**
  - Up to 1024 KB program flash memory on non-FlexMemory devices
  - Up to 512 KB program flash memory on FlexMemory devices
  - Up to 512 KB FlexNVM on FlexMemory devices
  - 16 KB FlexRAM on FlexMemory devices
  - Up to 128 KB RAM
  - Serial programming interface (EzPort)
  - FlexBus external bus interface
  - NAND flash controller interface

- **Clocks**
  - 3 to 32 MHz crystal oscillator
  - 32 kHz crystal oscillator
  - Multi-purpose clock generator

- **System peripherals**
  - Multiple low-power modes to provide power optimization based on application requirements
  - Memory protection unit with multi-master protection
  - 32-channel DMA controller, supporting up to 128 request sources
  - External watchdog monitor
  - Software watchdog
  - Low-leakage wakeup unit

- **Security and integrity modules**
  - Hardware CRC module to support fast cyclic redundancy checks
  - Hardware random-number generator
  - Hardware encryption supporting DES, 3DES, AES, MD5, SHA-1, and SHA-256 algorithms
  - 128-bit unique identification (ID) number per chip

- **Human-machine interface**
  - Low-power hardware touch sensor interface (TSI)
  - General-purpose input/output

- **Analog modules**
  - Four 16-bit SAR ADCs
  - Programmable gain amplifier (PGA) (up to x64) integrated into each ADC
  - Two 12-bit DACs
  - Four analog comparators (CMP) containing a 6-bit DAC and programmable reference input
  - Voltage reference

- **Timers**
  - Programmable delay block
  - Two 8-channel motor control/general purpose/PWM timers
  - Two 2-channel quadrature decoder/general
  - purpose timers
  - IEEE 1588 timers
  - Periodic interrupt timers
  - 16-bit low-power timer
  - Carrier modulator transmitter
  - Real-time clock

- **Communication interfaces**
  - Ethernet controller with MII and RMII interface to external PHY and hardware IEEE 1588 capability
  - USB high-/full-/low-speed On-the-Go controller with ULPI interface
  - USB high-/full-/low-speed On-the-Go controller with on-chip high speed transceiver
  - USB full-/low-speed On-the-Go controller with on-chip transceiver
  - USB Device Charger detect
  - Two Controller Area Network (CAN) modules
  - Three SPI modules
  - Two I2C modules
  - Six UART modules
  - Secure Digital host controller (SDHC)
  - Two I2S modules

4. Clock Distribution

The Multipurpose Clock Generator (MCG, [1]) module controls which clock source is used to derive the system clocks. The clock generation logic divides the selected clock source into a variety of clock domains, including the clocks for the system bus masters, system bus slaves, and flash memory. The clock generation logic also implements module-specific clock gating to allow granular shutoff of modules.

The primary clocks for the system are generated from the MCGOUTCLK clock. The clock generation circuitry provides several clock dividers that allow different portions of the device to be clocked at different frequencies. This allows for tradeoffs between performance and power dissipation. Various modules, such as the USB OTG Controller, have module-specific clocks that can be generated from the MCGPLLCLK or MCGFLLCLK clock. In addition, there are various other module-specific clocks that have other alternate sources. Clock selection for most modules is controlled by the SOPT registers in the SIM module. The clocking diagram for MCG module can be seen in detail in Fig 3.

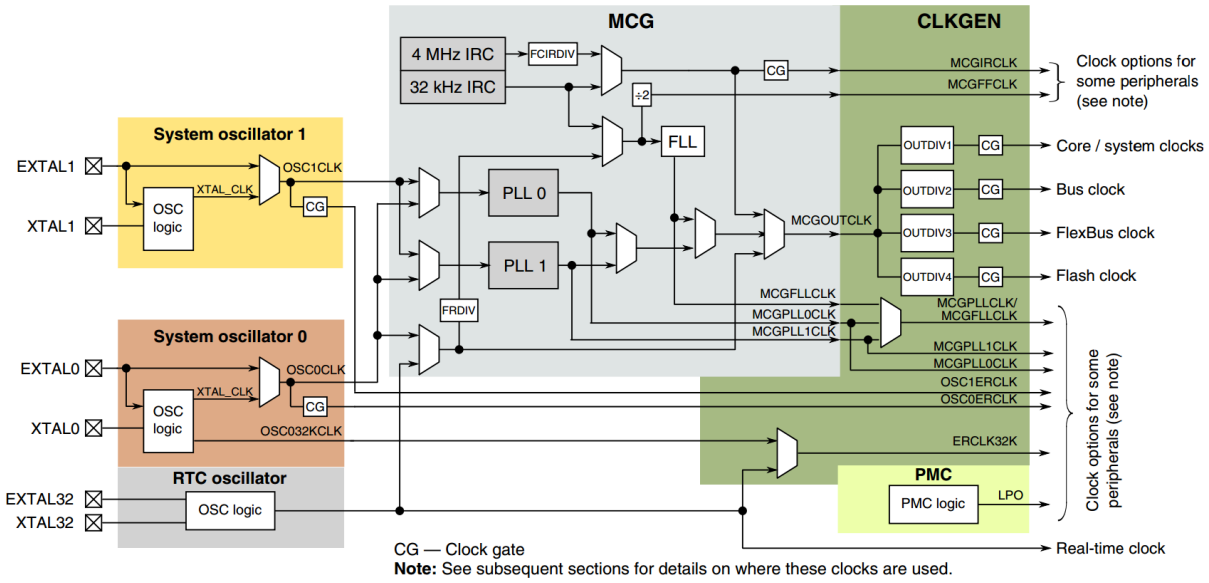


Fig 3 Clocking diagram

In addition to the MCG module, K60 possesses three additional clock modules [1]:

- **Oscillators (OSC)** – two high frequency crystal oscillators, which generate filtered oscillator clock signals - OSCCLK for MCU system, OSCERCLK for on-chip peripherals, and OSC32KCLK. On Bilbao Bizkaia minimodule, OSC is omitted and an external 50 MHz crystal oscillator (Q1) and a small set of necessary components is used as a clock source.
- **RTC Oscillator (RTC OSC)** – provides a clock source for the Real Time Clock (RTC) module. It is used in conjunction with an external 32 kHz crystal (Q2).

The following are a few of the more common clock configurations for this device:

	Option 1	Option 2
Core clock	120 MHz	150 MHz
System clock	120 MHz	150 MHz
Bus clock	60 MHz	75 MHz
FlexBus clock	40 MHz	50 MHz
Flash clock	20 MHz	25 MHz

5. Schematic and assembly

Module schematic is presented on page 9. The placement of components on top and bottom side of the module is shown in Fig 6 and Fig 7 respectively. The components needed to assemble the module are listed in Table 1.

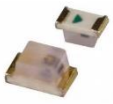
Components mounted on the board include: MK60FX512VLQ15 microcontroller in LQFP144 package (U1), a 50Mhz crystal oscillator (Q1) along with accompanying components (R1, R2 – 68 Ω), an 32kMHz oscillator (Q2), power supply filtering capacitors (C1, C2, C3 .. C18 – 100nF, C5 – 22uF), power supply filtering chokes (L1 .. L7 – 100MHz), micro USB B connector along with accompanying components (R4, R5 – 33Ω) and a safety diode D1.

Table 1 Bill of materials

Qty	Parts	Value	Package	Description
1	USB		SMD	micro USB connector
1	PWR		LED0603	LED
1	J-LINK		ML10	2x5 connector
2	SVL, SVR			2x24 pin header
1	SVT			2x13 pin header
7	L1, L2, L3, L4, L5, L6, L7	100MHz	M0805	inductor
12	C1, C2, C3, C4, C6, C8, C9, C10, C11, C13, C17, C18	100nF	C0603	capacitor
1	C15	10nF	C0603	capacitor
2	C14, C16	1uF	C0603	capacitor
1	C12	22uF	SMC B	polarized capacitor
1	R2	1k	R0603	resistor
2	R4, R5	33	R0603	resistor
2	R1, R3	68	R0603	resistor
1	R6	510	R0603	resistor
1	Q1	50MHz	DXO-57	crystal oscillator
1	Q2	32768Hz	2-POLE SMD	crystal
1	U1	MK60FX512VLQ15	LQFP144	Freescale Kinetis K60 microcontroler
1	D1		SOD523	schottky diode
1	J1		N/A	! NOT A PART

resistor

capacitor

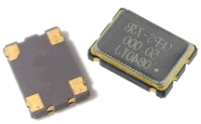


LED

inductor

polarized capacitor

diode



crystal oscillator

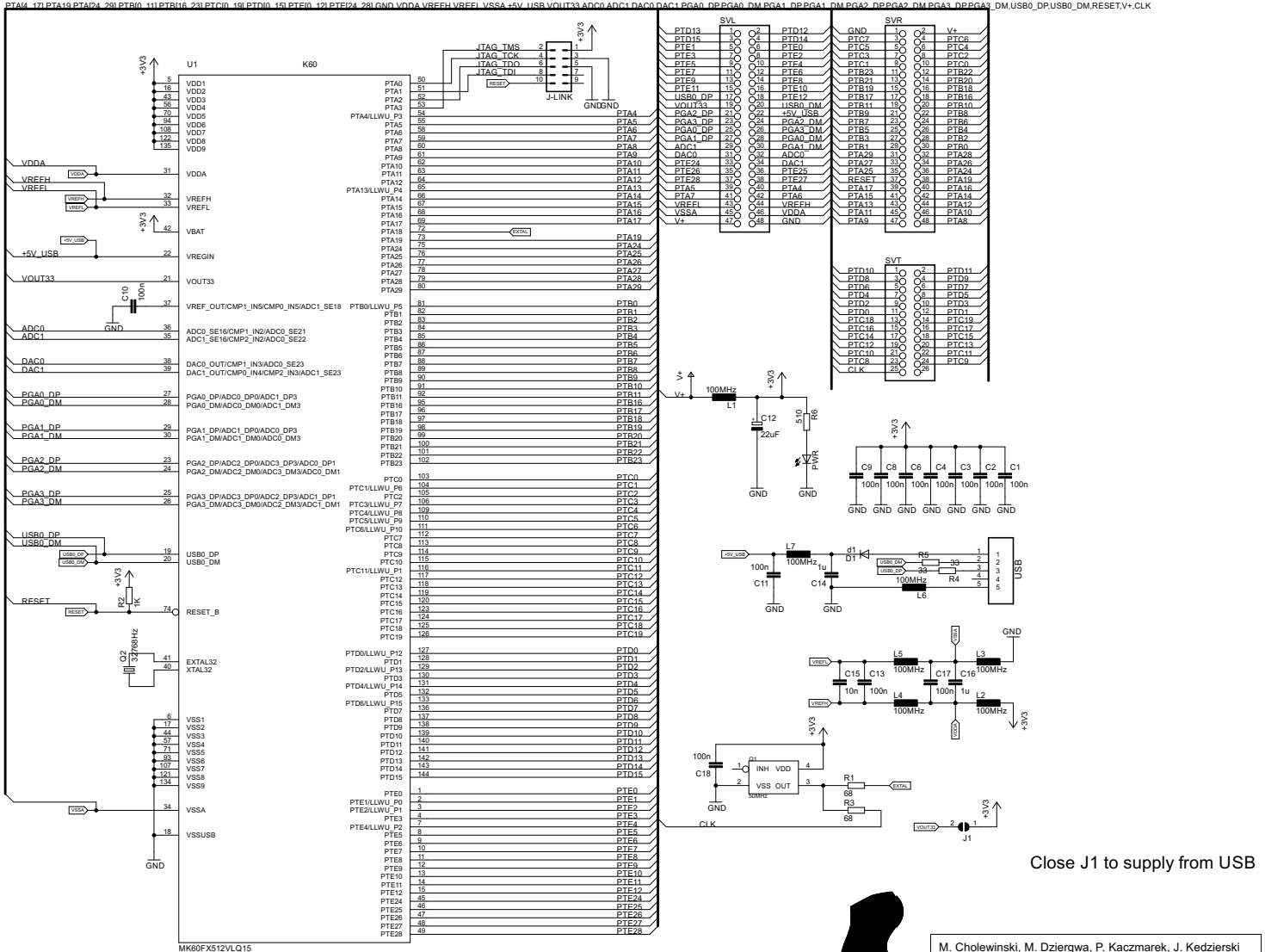
2-pole crystal

Freescale Kinetis K60

pin headers

2x5 connector

micro USB connector


PTA[4..17],PTA19,PTA[24..29],PTB[0..11],PTB[16..23],PTC[0..19],PTD[0..15],PTE[0..12],PTE[24..28],GND,VDDA,VREFH,VREFL,VSSA,+5V_USB,VOUT33,ADC0,ADC1,DAC0,DAC1,PGA0_DP,PGA0_DM,PGA1_DP,PGA1_DM,PGA2_DP,PGA2_DM,PGA3_DP,PGA3_DM,USB0_DP,USB0_DM,RESET,V+,CLK
U1
K60
MK60FX512VLQ15
SVL
SVR
SVT
J-LINK
JTAG_TMS
JTAG_TCK
JTAG_TDO
JTAG_TDI
RESET
Close J1 to supply from USB
M. Cholewinski, M. Dziergwa, P. Kaczmarek, J. Kedzierski
Wroclaw University of Technology
TITLE: K60_module
BILBAO Minimodule
Document Number:
REV:
Date: 2013-12-12 17:15:54
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BILBAO BIZKAIA
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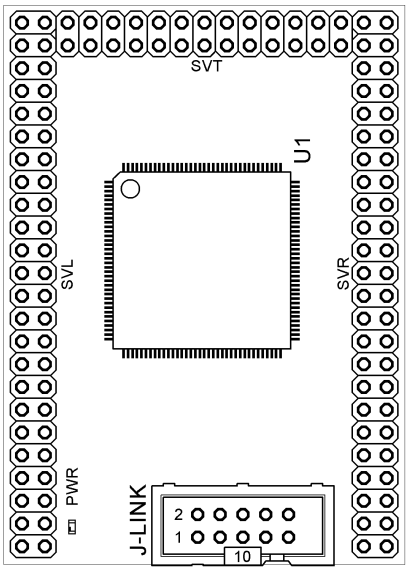

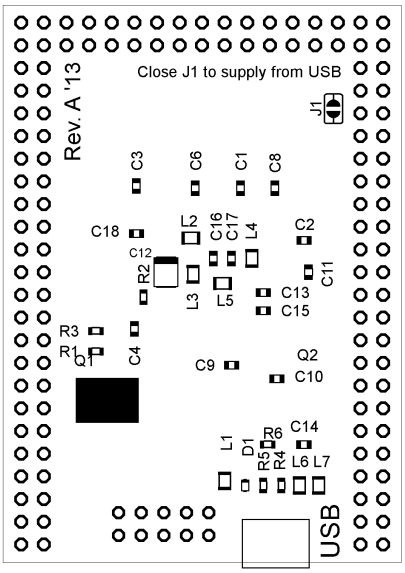

Fig 6 Placement of components - top

Fig 7 Placement of components - bottom

6. Power supply

The minimodule is powered from an external 3.3V power source. It is also possible to power the K60 microcontroller directly from USB. In order to achieve this, J1 jumper has to be shorted. This will cause the internal voltage regulator to be used to supply power to the MCU. **Please note that it is not allowed to exceed 290mA load**. **Also, when using USB to power the module DO NOT apply any other external power source to the module.** Moreover, the MCU peak current consumption can reach 300mA. This means that when the MCU is running at full speed it is impossible to power any devices from the internal voltage regulator.

7. Programming

The Bilbao Bizkaia minimodule can be programmed using a specialized interface such as the SEGGER J-Link [6], which is the most widely used line of debug probes available today, due to impressive performance, extensive feature set, large number of supported CPUs, and compatibility with all popular development environments. With up to 3 MBytes/s download speed to RAM and record breaking flashloaders, as well as the ability to set an unlimited number of breakpoints in flash memory of MCUs, the J-Link (Fig 8) debug probes are undoubtedly the best choice to optimize debugging and flash programming experience.

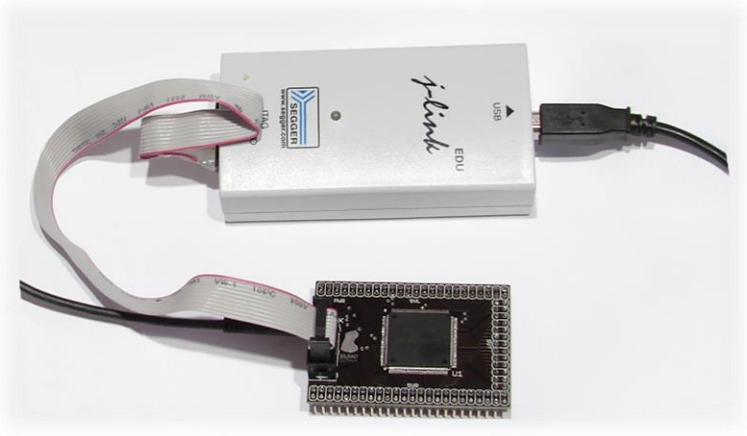

Fig 8 Bilbao Bizkaia minimodule connected to J-Link EDU

In order to start programming, the minimodule has to be connected to the programmer using an IDC connector. The module uses a 10 pin IDC socket and J-Link uses a 20 pin IDC socket. This dictates the need to use some form of an adapter, as shown in Fig 8. J-Link has to be connected to a PC, running software compatible with Freescale Kinetis MCUs such as CodeWarrior Development Studio [3] (at least version 10.X.), which features:

- Eclipse IDE,
- Build system with optimizing C/C++ compilers for RS08, HCS08, ARM, and ColdFire processors,
- Extensions to Eclipse C/C++ Development Tools (CDT) to provide sophisticated features to troubleshoot and repair embedded applications.

Another useful tool when beginning to work with Freescale microcontrollers is Processor Expert [4, 5], which is designed for rapid application development of embedded applications for a wide range of microcontrollers and microprocessor systems. It is integrated as a plug-in into the CodeWarrior IDE. Processor Expert generates code from the Embedded Components and CodeWarrior manages the project files, and compilation and debug processes.

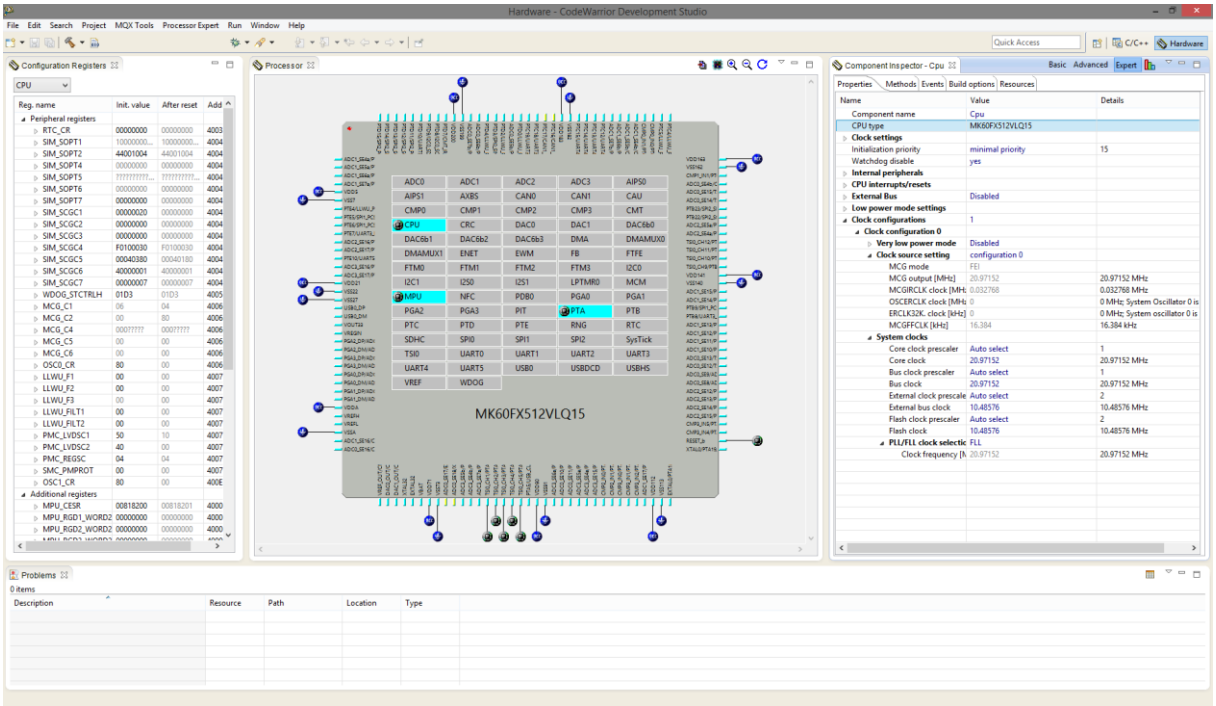

Fig 8 Processor Expert plug-in

In order to start working with a new project a project creation wizard is used. Choose **File**, then **New** and click **Bareboard Project**. A wizard window will show up where the project name and workspace path can be specified. Then, the following project options need to be configured:

- **Devices:** select *K60FX512 (150 Mhz)*,
- **Connections:** select (unless using a different programmer) *Segger J-Link / J-Trace / SWO (SWD based)*
- **Language and Build Tools Options**
  - **Language:** leave *C*,
  - **Floating Point:** leave *Hardware (-mfloat-abi=hard)*,
  - **ARM Build Tools:** select *Freescale*,
- **Rapid Aplication Development**
  - **Rapid Aplication Development:** select *Processor Expert*,
  - **Start with perspective designed for:** select *Hardware configuration*.

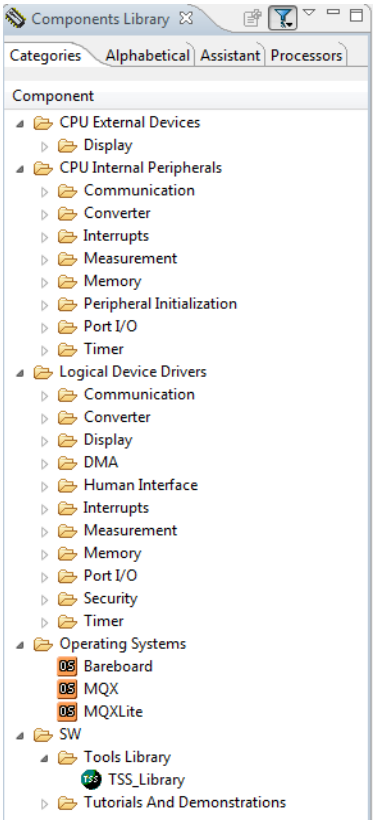

Fig 9 PE module categories

When a project is created Processor Expert automatically introduces one or more CPU modules. These can be adjusted to the user's needs via graphical user interface. After the CPU has been initialized, various new components can be added to the project. These are divided into the following categories project (Fig. 9):

- **CPU External Devices** – components for devices externally controlled to the CPU. For example sensors, memories, displays or EVM equipment,
- **CPU Internal Peripherals** – components using any of on-chip peripherals offered by the CPU,
- **Logical Device Drivers** – developed to offer users the Hardware Abstraction Layer (HAL) for bare-metal applications as well as RTOS applications,
- **Operating systems** – components related to Processor Expert interaction with operating system running on the target,
- **SW** – components encapsulating pure software algorithms or inheriting a hardware-dependent components for accessing peripherals.

After double-clicking on the selected component, PE will add it to the current project, and it will show up in the Components tab. Double-clicking a component added this way will open the configuration window for that module. Importantly, after each change in the module configuration, it has to be built again. Some configuration options may be unavailable, depending on how a certain block is set up. Unfortunately, Processor Expert does not allow to change all available registers/fields. In such situations it is advisable to use Peripheral Initialization modules, which provide only initialization configuration of a function block. These modules can be found in the Components library in Processor Internal Peripherals/Peripheral Initialization section. More detailed information on configuring and adding components can be found in [5] (K40 and K60 microcontrollers can be configured using PE in an almost identical manner)

8. Connectors and signals

In order to allow the user to utilize the full capabilities of the K60 microcontroller, all the signals have been connected to two row pin headers (SVL, SVT, SVR). This allows for a fast and reliable connection to another, custom designed board. Numbering and spacing of the pins is shown in Fig 10. A detailed description of pins and along with their various functions is presented in Table 2, Table 3 and Table 4.

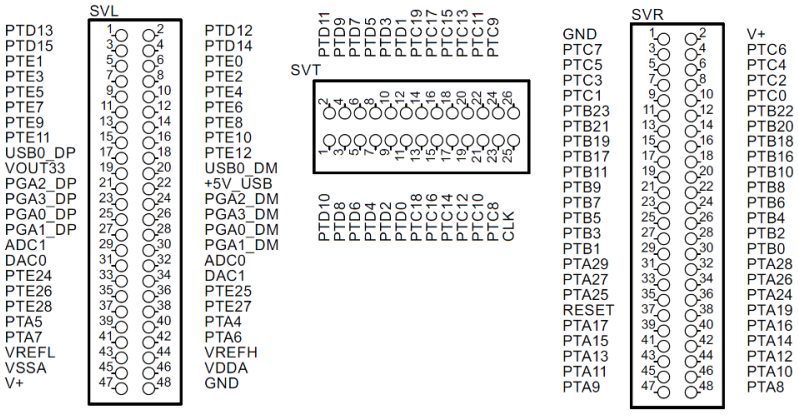

Fig 10 Pin header overview

Table 2 SVL Connector

	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
1	**PTD13**	DISABLED		PTD13	SPI2_SOUT		SDHC0_D5		FB_A21	
2	**PTD12**	DISABLED		PTD12	SPI2_SCK	FTM3_FLT0	SDHC0_D4		FB_A20	
3	**PTD15**	DISABLED		PTD15	SPI2_PCS1		SDHC0_D7		FB_A23	
4	**PTD14**	DISABLED		PTD14	SPI2_SIN		SDHC0_D6		FB_A22	
5	**PTE1**	ADC1_SE5a	ADC1_SE5a	PTE1/ LLWU_P0	SPI1_SOUT	UART1_RX	SDHC0_D0		I2C1_SCL	SPI1_SIN
6	**PTE0**	ADC1_SE4a	ADC1_SE4a	PTE0	SPI1_PCS1	UART1_TX	SDHC0_D1		I2C1_SDA	RTC_CLKOUT
7	**PTE3**	ADC1_SE7a	ADC1_SE7a	PTE3	SPI1_SIN	UART1_RTS_ b	SDHC0_CMD			SPI1_SOUT
8	**PTE2**	ADC1_SE6a	ADC1_SE6a	PTE2/ LLWU_P1	SPI1_SCK	UART1_CTS_ b	SDHC0_DCLK			
9	**PTE5**	DISABLED		PTE5	SPI1_PCS2	UART3_RX	SDHC0_D2		FTM3_CH0	
10	**PTE4**	DISABLED		PTE4/ LLWU_P2	SPI1_PCS0	UART3_TX	SDHC0_D3			
11	**PTE7**	DISABLED		PTE7		UART3_RTS_ b	I2S0_RXD0		FTM3_CH2	
12	**PTE6**	DISABLED		PTE6	SPI1_PCS3	UART3_CTS_ b	I2S0_MCLK		FTM3_CH1	USB_SOF_ OUT
13	**PTE9**	ADC2_SE17	ADC2_SE17	PTE9	I2S0_TXD1	UART5_RX	I2S0_RX_ BCLK		FTM3_CH4	
14	**PTE8**	ADC2_SE16	ADC2_SE16	PTE8	I2S0_RXD1	UART5_TX	I2S0_RX_FS		FTM3_CH3	
15	**PTE11**	ADC3_SE16	ADC3_SE16	PTE11		UART5_RTS_ b	I2S0_TX_FS		FTM3_CH6	
16	**PTE10**	DISABLED		PTE10		UART5_CTS_ b	I2S0_TXD0		FTM3_CH5	
17	**USB0_DP**	USB0_DP	USB0_DP							
18	**PTE12**	ADC3_SE17	ADC3_SE17	PTE12			I2S0_TX_ BCLK		FTM3_CH7	
19	**V_OUT33**	VOUT33	VOUT33							
20	**USB0_DM**	USB0_DM	USB0_DM							
21	**PGA2_DP**	PGA2_DP/ ADC2_DP0/ ADC3_DP3/ ADC0_DP1	PGA2_DP/ ADC2_DP0/ ADC3_DP3/ ADC0_DP1							
22	**+5V_USB**									
23	**PGA3_DP**	PGA3_DP/ ADC3_DP0/ ADC2_DP3/ ADC1_DP1	PGA3_DP/ ADC3_DP0/ ADC2_DP3/ ADC1_DP1							
24	**PGA2_DM**	PGA2_DM/ ADC2_DM0/ ADC3_DM3/ ADC0_DM1	PGA2_DM/ ADC2_DM0/ ADC3_DM3/ ADC0_DM1							
25	**PGA0_DP**	PGA0_DP/ ADC0_DP0/ ADC1_DP3	PGA0_DP/ ADC0_DP0/ ADC1_DP3							
26	**PGA3_DM**	PGA3_DM/ ADC3_DM0/ ADC2_DM3/ ADC1_DM1	PGA3_DM/ ADC3_DM0/ ADC2_DM3/ ADC1_DM1							
27	**PGA1_DP**	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DP/ ADC1_DP0/ ADC0_DP3							
28	**PGA0_DM**	PGA1_DM/ ADC1_DM0/ ADC0_DM3	PGA1_DM/ ADC1_DM0/ ADC0_DM3							
29	**ADC1**	ADC1_SE16/ CMP2_IN2/ ADC0_SE22	ADC1_SE16/ CMP2_IN2/ ADC0_SE22							
30	**PGA1_DM**	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DP/ ADC1_DP0/ ADC0_DP3							
31	**DAC0**	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23							
32	**ADC0**	ADC0_SE16/ CMP1_IN2/ ADC0_SE21	ADC0_SE16/ CMP1_IN2/ ADC0_SE21							
33	**PTE24**	ADC0_SE17/ EXTAL1	ADC0_SE17/ EXTAL1	PTE24	CAN1_TX	UART4_TX	I2S1_TX_FS		EWM_OUT_b	I2S1_RXD1
34	**DAC1**	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23							
35	**PTE26**	ADC3_SE5b	ADC3_SE5b	PTE26	ENET_1588_ CLKIN	UART4_CTS_ b	I2S1_TXD0		RTC_CLKOUT	USB_CLKIN
36	**PTE25**	ADC0_SE18/ XTAL1	ADC0_SE18/ XTAL1	PTE25	CAN1_RX	UART4_RX	I2S1_TX_ BCLK		EWM_IN	I2S1_TXD1

37	**PTE28**	ADC3_SE7a	ADC3_SE7a	PTE28						
38	**PTE27**	ADC3_SE4b	ADC3_SE4b	PTE27		UART4_RTS_ b	I2S1_MCLK			
39	**PTA5**	DISABLED		PTA5	USB_CLKIN	FTM0_CH2	RMII0_RXER/ MII0_RXER	CMP2_ OUT	I2S0_TX_ BCLK	JTAG_TRST_ b
40	**PTA4**	NMI_b/ EZP_CS_b	TSI0_CH5	PTA4/ LLWU_P3		FTM0_CH1				NMI_b
41	**PTA7**	ADC0_SE10	ADC0_SE10	PTA7	ULPI_DIR	FTM0_CH4	I2S1_RX_ BCLK			TRACE_D3
42	**PTA6**	ADC3_SE6a	ADC3_SE6a	PTA6	ULPI_CLK	FTM0_CH3	I2S1_RXD0			TRACE_ CLKOUT
43	**VREFL**	VREFL	VREFL							
44	**VREFH**	VREFH	VREFH							
45	**VSSA**	VSSA	VSSA							
46	**VDDA**	VDDA	VDDA							
47	**V+**									
48	**GND**									

Table 3 SVT Connector

	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
1	**PTD10**	DISABLED		PTD10		UART5_RTS_ b			FB_A18/ NFC_RE	
2	**PTD11**	DISABLED		PTD11	SPI2_PCS0	UART5_CTS_ b	SDHC0_ CLKIN		FB_A19	
3	**PTD8**	DISABLED		PTD8	I2C0_SCL	UART5_RX			FB_A16/ NFC_CLE	
4	**PTD9**	DISABLED		PTD9	I2C0_SDA	UART5_TX			FB_A17/ NFC_ALE	
5	**PTD6**	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6	FB_AD0	FTM0_FLT0	
6	**PTD7**	DISABLED		PTD7	CMT_IRO	UART0_TX	FTM0_CH7		FTM0_FLT1	
7	**PTD4**									
8	**PTD5**	ADC0_SE6b	ADC0_SE6b	PTD5	SPI0_PCS2	UART0_CTS_b/ UART0_COL_ b	FTM0_CH5	FB_AD1/ NFC_DATA0	EWM_OUT_b	
9	**PTD2**	DISABLED		PTD2/	SPI0_SOUT	UART2_RX	FTM3_CH2	FB_AD4	I2S1_RX_FS	
10	**PTD3**	DISABLED		PTD3	SPI0_SIN	UART2_TX	FTM3_CH3	FB_AD3	I2S1_RX_ BCLK	
11	**PTD0**	DISABLED		PTD0/	SPI0_PCS0	UART2_RTS_ b	FTM3_CH0	FB_ALE/	I2S1_RXD1	
12	**PTD1**	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK	UART2_CTS_ b	FTM3_CH1	FB_CS0_b	I2S1_RXD0	ADC0_SE5b
13	**PTC18**	DISABLED		PTC18		UART3_RTS_ b	ENET0_1588 _ TMR2	FB_TBST_b/ FB_CS2_b/ FB_BE15_8_b	NFC_CE1_b	
14	**PTC19**	DISABLED		PTC19		UART3_CTS_ b	ENET0_1588 _ TMR3	FB_CS3_b/ FB_BE7_0_b	FB_TA_b	
15	**PTC16**	DISABLED		PTC16	CAN1_RX	UART3_RX	ENET0_1588 _ TMR0	FB_CS5_b/ FB_TSIZ1/ FB_BE23_16_b	NFC_RB	
16	**PTC17**	DISABLED		PTC17	CAN1_TX	UART3_TX	ENET0_1588 _ TMR1	FB_CS4_b/ FB_TSIZ0/ FB_BE31_24_b	NFC_CE0_b	
17	**PTC14**	DISABLED		PTC14		UART4_RX		FB_AD25		
18	**PTC15**	DISABLED		PTC15		UART4_TX		FB_AD24		
19	**PTC12**	DISABLED		PTC12		UART4_RTS_ b		FB_AD27	FTM3_FLT0	
20	**PTC13**	DISABLED		PTC13		UART4_CTS_ b		FB_AD26		
21	**PTC10**	ADC1_SE6b	ADC1_SE6b	PTC10	I2C1_SCL	FTM3_CH6	I2S0_RX_FS	FB_AD5/ NFC_DATA2	I2S1_MCLK	
22	**PTC11**	ADC1_SE7b	ADC1_SE7b	PTC11/ LLWU_P11	I2C1_SDA	FTM3_CH7	I2S0_RXD1	FB_RW_b/ NFC_WE		
23	**PTC8**	ADC1_SE4b/ CMP0_IN2	ADC1_SE4b/ CMP0_IN2	PTC8		FTM3_CH4	I2S0_MCLK	FB_AD7/ NFC_DATA4		
24	**PTC9**	ADC1_SE5b/ CMP0_IN3	ADC1_SE5b/ CMP0_IN3	PTC9		FTM3_CH5	I2S0_RX_ BCLK	FB_AD6/ NFC_DATA3	FTM2_FLT0	
25	**CLK**									
26	**----**									

Table 4 SVR Connector

	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
1	**GND**									
2	**V+**									
3	**PTC7**	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN	USB_SOF_ OUT	I2S0_RX_FS	FB_AD8/ NFC_DATA5		
4	**PTC6**	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P1 0	SPI0_SOUT	PDB0_EXTRG	I2S0_RX_ BCLK	FB_AD9/ NFC_DATA6	I2S0_MCLK	
5	**PTC5**	DISABLED		PTC5/	SPI0_SCK	LPTMR0_ ALT2	I2S0_RXD0	FB_AD10/ NFC_DATA7	CMP0_OUT	I2S1_TX_FS
6	**PTC4**	DISABLED		PTC4/	SPI0_PCS0	UART1_TX	FTM0_CH3	FB_AD11/ NFC_DATA8	CMP1_OUT	I2S1_TX_ BCLK
7	**PTC3**	CMP1_IN1	CMP1_IN1	PTC3/ LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT	I2S0_TX_ BCLK	
8	**PTC2**	ADC0_SE4b/ CMP1_IN0/ TSI0_CH15	ADC0_SE4b/ CMP1_IN0/ TSI0_CH15/	PTC2	SPI0_PCS2	UART1_CTS_ b	FTM0_CH1	FB_AD12/ NFC_DATA9	I2S0_TX_FS	
9	**PTC1**	ADC0_SE15/ TSI0_CH14	ADC0_SE15/ TSI0_CH14	PTC1/ LLWU_P6	SPI0_PCS3	UART1_RTS_ b	FTM0_CH0	FB_AD13/	I2S0_TXD0	
10	**PTC0**	ADC0_SE14/ TSI0_CH13	ADC0_SE14/ TSI0_CH13	PTC0	SPI0_PCS4	PDB0_EXTRG		FB_AD14/ NFC_DATA11	I2S0_TXD1	
11	**PTB23**	DISABLED		PTB23	SPI2_SIN	SPI0_PCS5		FB_AD28/ NFC_DATA12	CMP3_OUT	
12	**PTB22**	DISABLED		PTB22	SPI2_SOUT			FB_AD29/ NFC_DATA13	CMP2_OUT	
13	**PTB21**	ADC2_SE5a	ADC2_SE5a	PTB21	SPI2_SCK			FB_AD30/ NFC_DATA14	CMP1_OUT	
14	**PTB20**	ADC2_SE4a	ADC2_SE4a	PTB20	SPI2_PCS0			FB_AD31/ NFC_DATA15	CMP0_OUT	ADC2_SE4a
15	**PTB19**	TSI0_CH12	TSI0_CH12	PTB19	CAN0_RX	FTM2_CH1	I2S0_TX_FS	FB_OE_b	FTM2_QD_ PHB	
16	**PTB18**	TSI0_CH11	TSI0_CH11	PTB18	CAN0_TX	FTM2_CH0	I2S0_TX_ BCLK	FB_AD15	FTM2_QD_ PHA	
17	**PTB17**	TSI0_CH10	TSI0_CH10	PTB17	SPI1_SIN	UART0_TX	I2S1_TXD1	FB_AD16	EWM_OUT_b	
18	**PTB16**	TSI0_CH9	TSI0_CH9	PTB16	SPI1_SOUT	UART0_RX	I2S1_TXD0	FB_AD17	EWM_IN	
19	**PTB11**	ADC1_SE15	ADC1_SE15	PTB11	SPI1_SCK	UART3_TX	I2S1_TX_FS	FB_AD18	FTM0_FLT2	
20	**PTB10**	ADC1_SE14	ADC1_SE14	PTB10	SPI1_PCS0	UART3_RX	I2S1_TX_ BCLK	FB_AD19	FTM0_FLT1	
21	**PTB9**	DISABLED		PTB9	SPI1_PCS1	UART3_CTS_ b		FB_AD20		
22	**PTB8**	DISABLED		PTB8		UART3_RTS_ b		FB_AD21		
23	**PTB7**	ADC1_SE13	ADC1_SE13	PTB7				FB_AD22		
24	**PTB6**	ADC1_SE12	ADC1_SE12	PTB6				FB_AD23		
25	**PTB5**	ADC1_SE11	ADC1_SE11	PTB5			ENET0_1588 _TMR3		FTM2_FLT0	
26	**PTB4**	ADC1_SE10	ADC1_SE10	PTB4			ENET0_1588 _TMR2		FTM1_FLT0	
27	**PTB3**	ADC0_SE13/ TSI0_CH8	ADC0_SE13/ TSI0_CH8	PTB3	I2C0_SDA	UART0_CTS_b/ UART0_COL_ b	ENET0_1588 _TMR1		FTM0_FLT0	
28	**PTB2**	ADC0_SE12/ TSI0_CH7	ADC0_SE12/ TSI0_CH7	PTB2	I2C0_SCL	UART0_RTS_ b	ENET0_1588 _TMR0		FTM0_FLT3	
29	**PTB1**	ADC0_SE9/ ADC1_SE9/ ADC2_SE9/ ADC3_SE9/ TSI0_CH6	ADC0_SE9/ ADC1_SE9/ ADC2_SE9/ ADC3_SE9/ TSI0_CH6	PTB1	I2C0_SDA	FTM1_CH1	RMII0_MDC/ MII0_MDC		FTM1_QD_ PHB	
30	**PTB0**	ADC0_SE8/ ADC1_SE8/ ADC2_SE8/ ADC3_SE8/ TSI0_CH0	ADC0_SE8/ ADC1_SE8/ ADC2_SE8/ ADC3_SE8/ TSI0_CH0	PTB0/	I2C0_SCL	FTM1_CH0	RMII0_MDI/ MII0_MDIO		FTM1_QD_ PHA	
31	**PTA29**	ADC2_SE12	ADC2_SE12	PTA29	ULPI_DATA7		MII0_COL		FB_A24	
32	**PTA28**	ADC2_SE13	ADC2_SE13	PTA28	ULPI_DATA6		MII0_TXER		FB_A25	
33	**PTA27**	ADC2_SE14	ADC2_SE14	PTA27	ULPI_DATA5		MII0_CRS		FB_A26	
34	**PTA26**	ADC2_SE15	ADC2_SE15	PTA26	ULPI_DATA4		MII0_TXD3		FB_A27	
35	**PTA25**	CMP3_IN5	CMP3_IN5	PTA25	ULPI_DATA3		MII0_TXCLK		FB_A28	
36	**PTA24**	CMP3_IN4	CMP3_IN4	PTA24	ULPI_DATA2		MII0_TXD2		FB_A29	
37	**RESET**	RESET_b	RESET_b							
38	**PTA19**	XTAL0	XTAL0	PTA19		FTM1_FLT0	FTM_CLKIN1		LPTMR0_ ALT1	
39	**PTA17**	ADC1_SE17	ADC1_SE17	PTA17	SPI0_SIN	UART0_RTS_ b	RMII0_TXD1/ MII0_TXD1		I2S0_MCLK	
40	**PTA16**	CMP3_IN2	CMP3_IN2	PTA16	SPI0_SOUT	UART0_CTS_b/ UART0_COL_ b	RMII0_TXD0/ MII0_TXD0		I2S0_RX_FS	I2S0_RXD1

41	**PTA15**	CMP3_IN1	CMP3_IN1	PTA15	SPI0_SCK	UART0_RX	RMII0_TXEN/ MII0_TXEN	I2S0_RXD0	
42	**PTA14**	CMP3_IN0	CMP3_IN0	PTA14	SPI0_PCS0	UART0_TX	RMII0_CRS_	I2S0_RX_ BCLK	I2S0_TXD1
43	**PTA13**	CMP2_IN1	CMP2_IN1	PTA13/ LLWU_P4	CAN0_RX	FTM1_CH1	RMII0_RXD0/ MII0_RXD0	I2S0_TX_FS	FTM1_QD_ PHB
44	**PTA12**	CMP2_IN0	CMP2_IN0	PTA12	CAN0_TX	FTM1_CH0	RMII0_RXD1/ MII0_RXD1	I2S0_TXD0	FTM1_QD_ PHA
45	**PTA11**	ADC3_SE15	ADC3_SE15	PTA11	ULPI_DATA1	FTM2_CH1	MII0_RXCLK	FTM2_QD_ PHB	
46	**PTA10**	ADC3_SE4a	ADC3_SE4a	PTA10	ULPI_DATA0	FTM2_CH0	MII0_RXD2	FTM2_QD_ PHA	TRACE_D0
47	**PTA9**	ADC3_SE5a	ADC3_SE5a	PTA9	ULPI_STP	FTM1_CH1	MII0_RXD3	FTM1_QD_ PHB	TRACE_D1
48	**PTA8**	ADC0_SE11	ADC0_SE11	PTA8	ULPI_NXT	FTM1_CH0	I2S1_RX_FS	FTM1_QD_ PHA	TRACE_D2

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